THE FUTURE OF PACKAGING

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INTRODUCTION

Virtually every electronic device must connect to an electronic system by means of an electromechanical structure called the package. The electronic component package concept has been in use for more than a century and electronics would not exist without the "package". Electronics can be divided into a simple hierarchy consisting of devices, packages, printed circuit boards (PCB) and a system. The package is the interface between the electronic device, such as a computer chip, and the PCB, that typically supports a group of packaged active and passive electronics. Devices are made from semiconductor materials; silicon is the dominant material, but includes compound semiconductors (composed of two or more chemical elements). While silicon is standard for logic and memory, compound semiconductors are used for LEDs, lasers, optoelectronics, and some RF chips.

Semiconductor devices are fabricated using a series of processes carried out in vacuum chambers, and in highly controlled and ultra-clean atmospheres, using mostly automatic equipment in fabs costing billions of dollars. Device feature sizes for the densest chips are now in the nano-scale range (1 to 100-nanometer; nm = 1-billionth of a meter) so that hundreds of millions of transistors can be formed on a single postage-stamp size chip. The semiconductor industry continues to increase density in several ways that include reducing sub-element dimensions, adding layers and moving to more "vertical" orientation.

Circuitry followed a different path. The printed circuit board industry continues to use basic "metal chemistry"; etching, plating and combinations that can be traced back to the 19^{th} and 20^{th} centuries [1]. Circuitry has been with us for over a century, but fundamental processes have only undergone modest changes. "Modern" photolithography was borrowed from the printing plate industry, for example. Regardless of the PCB process, the result is a pattern of metal traces, or tracks, on and within, a dielectric medium typically made of epoxy composite with glass reinforcement for mechanical stability. While there has certainly been progress in making finer traces and smaller vertical connections to achieve higher circuit density, the PCB industry has lagged behind the larger, more profitable, and better financed semiconductor industry. It is no surprise that semiconductor density continues to advance at a faster pace than that for PCBs. Electronic devices add more and more I/Os (input/output), often in a smaller area. The challenge of connecting devices to boards continues to increase. So what's the solution to the *density disparity dilemma*?

The component package is the *bridge* between the extremely dense device and the less dense PCB. The package also protects the device and interconnect, but may perform a dozen or more other functions. But enabling the electrical connections between chip and board is paramount task of the package.

EVOLUTION OF PACKAGING

The earliest packages were hermetic glass enclosures that were initially developed for optical/electronic ray constructions like Crookes and Geissler tubes requiring vacuum and special gasses to function. The first strategic device came a few years later as the 1897 Braun Tube that became the cathode ray tube (CRT), still the dominant display component today. The advent of wireless communications and vacuum tube amplifiers led to the vacuum tube as the standard package. Tube components could be plugged into sockets mounted on PCBs. The tubes were also made with metal and ceramics, but glass remained popular because "dead" tubes could be quickly spotted since they lacked a glowing filament.

But the solid-state break-through over 50-years ago would change electronics, packaging and the world forever. The invention of the transistor, followed by the development of interconnection methods for building integrated circuits (IC), was disruptive technology at its best. The IC produced a massive paradigm shift in the electronics industry, especially packaging. Not only was the IC orders of magnitude smaller and denser, it did not require a vacuum. This meant that the full-hermetic package could be discarded for more cost-effective alternatives, like plastics. The plastic package was introduced just prior to 1950 (see Figure 1).

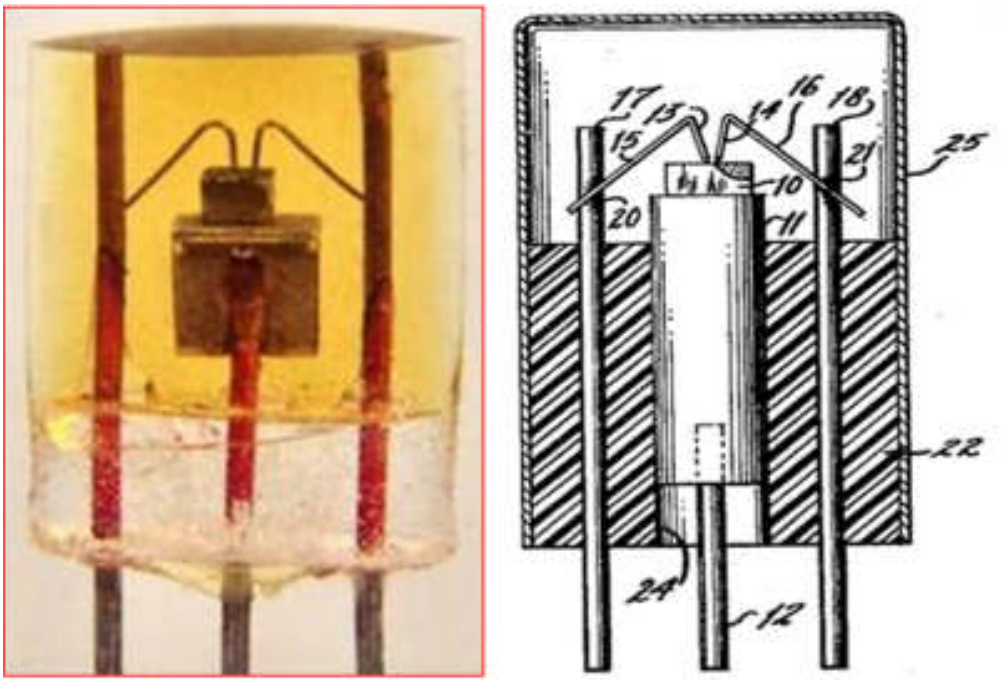

Figure 1 - First Plastic Package [ref. 2]

The Center of the High Tech Universe

The component package is at the virtual center of our high tech universe positioned between chips and PCBs. The package must accommodate the latest electronic devices and newer types, like MEMS (Micro-electro-mechanical-systems) and optical sensors. Each device can have different requirements making the package *device-specific*. But the

other side of this universe is applications. The package can also be *application-specific*. A memory package for a cell phone will have very different requirements than one for a desktop computer. The package is thus at the intersect of new devices and new applications as depicted in Figure 2.

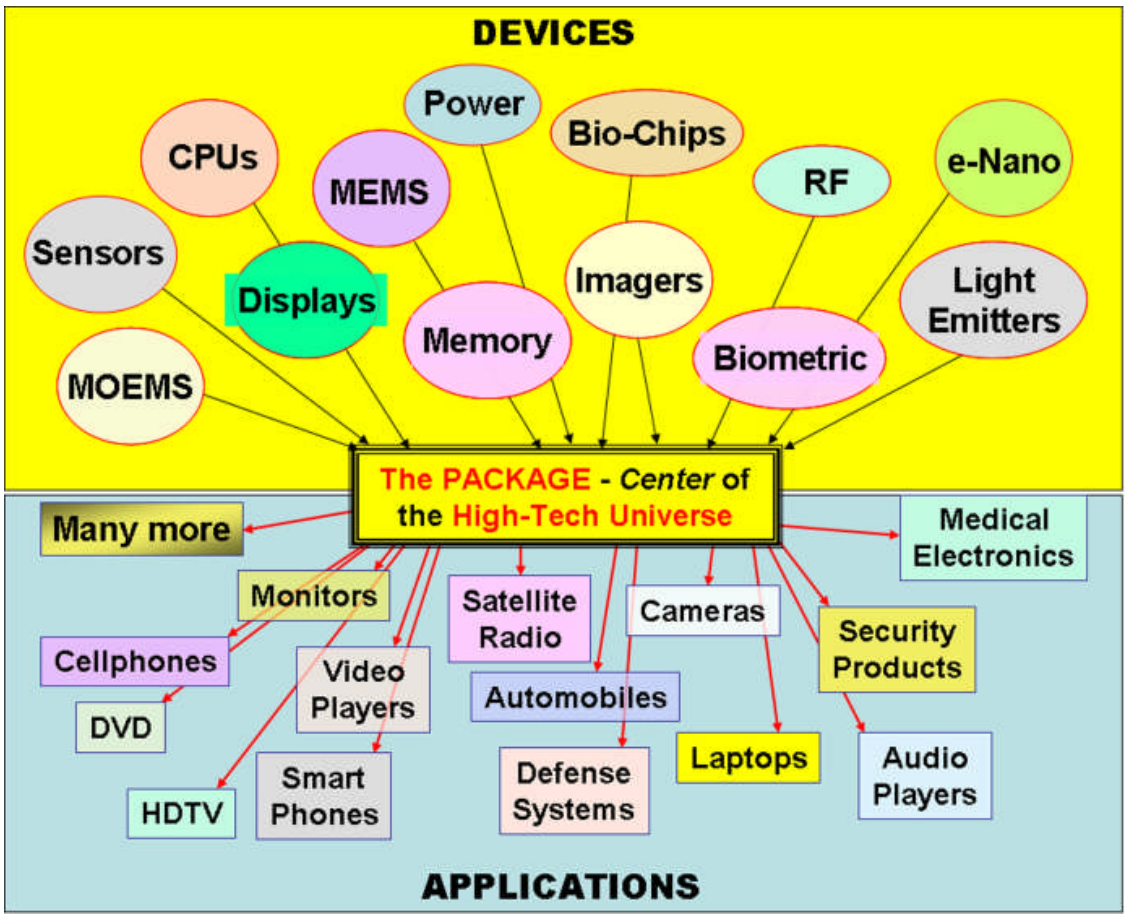

Figure 2 - Center of Technology Diagram

New Devices Packaging Challenges

The device determines the basic requirements for the package, especially the I/O interface that has been predominately electrical. The device can also set the hermeticity requirements. Mechanics has been incorporated into device called MEMS, adding a new set of requirements to deal with mechanical motion. Although photonic devices have been around for a long time, the proliferation of digital cameras has increased packaging challenges. The integration of optics into MEMS devices, called optical-MEMS, or MOEMS, lays on another set of needs to those already required for mechanical and electrical functions. And if that weren't already enough, breakthroughs in merging standard silicon electronics with photonic transmission technology (modulated signal lasers), promises, or threatens, to change the fundamental package. Silicon Photonics (Intel and UC-Santa Barbara) that will use "light" as the signal carrier, will need a package that can deal with light beams or perhaps optical fiber as we move away from copper as the transmission line [3].

New Products Packaging Challenges

We've been on a path to a "wearable electronics" form factor for personal products for decades and the phenomenal success is reflected in the fact that the cellphone has replaced the computer as the most important driver. Small yet powerful wearable products require extreme miniaturization resulting in entirely new package designs. But product and technology convergence has been part of the trend toward product miniaturization and this has created significant challenges and opportunities for packaging. So, what are the results?

PACKAGING TRENDS

Super Stacks - What's next in 3D?

The dual demand of "smaller, but more powerful", has dramatically affected memory devices and packaging. Memory is at the heart of many wearable products especially those aimed at entertainment. Media players (MP3, iPod, mobile-TV, etc.) are the ultimate "memory hogs". The semiconductor industry has done a remarkable job of memory chip densification, but product demand has outpaced what a single chip can offer. The package had already achieved chip-scale dimensions so "stacking" was the obvious strategy for densification at the package level. But there were, and still are, many approaches that include package-on-package (PoP), folded stacks (flex-based), pyramid stacks (progressively smaller chip-on-chip), and Chip-to-Chip (C2C) - directly stacked chips. Today, cell phones and media players use all of these packages, except C2C, that isn't available yet.

Chip and package stacking will certainly continue, but how will it evolve? Debates continue over PoP vs. multi-chip packages (MCP), but both have their place and will continue. Chips with lower yields favor PoP, but extreme density/performance fits MCP. It all comes down to technology. While the older pyramid stack, sometimes called "wedding cake", allows existing processes and equipment to be used, it lacks high volumetric efficiency. Chip-to-Chip stacking appears to be the next step for high-density packaging judging from press releases and patent applications. While direct-chip bonding should offer the highest density and performance, the jury is still out on cost. Most C2C strategies require through-vias that must be plated or somehow made conductive. Next, chips must be aligned and bonded together to form reliable electrical connections. Finally, an assembly interface is needed, perhaps forming bumps. Figure 3 shows a stack with a flip chip base and wafer-level underfill (WUF). While it's too early to tell how the MCP battles will play out, C2C will likely be commercialized in 2007.

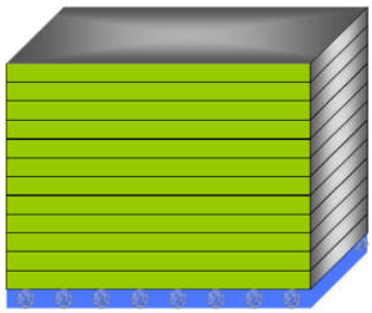

Figure 3 - Chip-to-Chip (C2C)

Opto Inside

In the past, optical chips and packages have been mostly a low-volume area, often utilizing specialized and expensive metal or ceramic fully hermetic packages. But the *Digital Photo Revolution* changed this. Most cell phones have cameras with picture quality approaching moderately priced stand-alone cameras. The package for the photo-imaging chip must be small and economical, but not necessarily hermetic. CMOS photo chips, the most popular low-to-mid level device, can be packaged in simple CSP format, such as the packages developed by Shellcase (acquired by Tessera Technologies). The trend for optical devices is System-in-Package (SiP) where supporting electronics and optics is all contained in one efficient package.

SiP - Density and Performance with Cost-Reduction

System-in-Package is increasingly popular; an active chip and supporting passive components, or a suite of active devices and components, is configured in a single package to produce a more efficient system providing a total-, or sub-function. Examples include cell phone multi-band transmitters, other wireless modules, like Bluetooth, single-package power controller/converters, and camera modules. SiP benefits include higher density, smaller circuit boards, and higher performance, especially for RF, higher reliability, ability to use chips from different sources, faster time-to-market, and reduced total cost. Integrated MEMS products, such as self-powered sensors with wireless linking, will adopt SiP. But future MEMS-based products, like turbines and rocket engines, may evolve to a level where the package and device are one.

Wafer-Level Packaging (WLP)

Wafer-Level Packaging, while relatively new, has been used by the MEMS industry for over a decade. In fact, cost-effective inertial sensors, such as the devices used in vehicle air bags, would probably not be practical without WLP, or more precisely, “WL-pre-packaging”. MEMS devices have two special requirements in addition to all of the standard requirements for electronic devices. Mechanical motion can’t be restricted - most MEMS devices have moving parts. Conventional epoxy overmolding would “lock” the mechanical structure making the process unacceptable. MEMS must also be protected from micro-contamination; a single tiny particle can become “sand in the gears” that impedes movement. Sawing residue, easily removed from standard electronics chips, wrecks most MEMS chips.

One elegant solution is to cap the active area of the MEMS chips using a wafer-level process. A wafer of etched caps is bonded to the MEMS wafer, by one of a half-dozen available methods, although glass frit bonding is the most popular. The cap wafer is typically singulated after wafer bonding to expose MEMS pads for wire bonding. The MEMS wafer can now be singulated without concern for contamination since the cap keeps the mechanical zone free of particles. The capped MEMS chips can now be packaged using standard wire bond and overmolding. The *cap-bond-mold* strategy is used for accelerometers and gyroscopes, but isn’t applicable to optical and fluidic MEMS. But, the wafer capping, using passive caps, appears to be an interim step with too many steps.

We can expect to see MEMS move to full-WLP in the near future. There are two contending approaches: protective caps with electrical vias that mate with MEMS chip pads, and MEMS chips with through-vias. A recent review of US patent applications favors caps with electrical interconnect structures. Figure 4 shows one example.

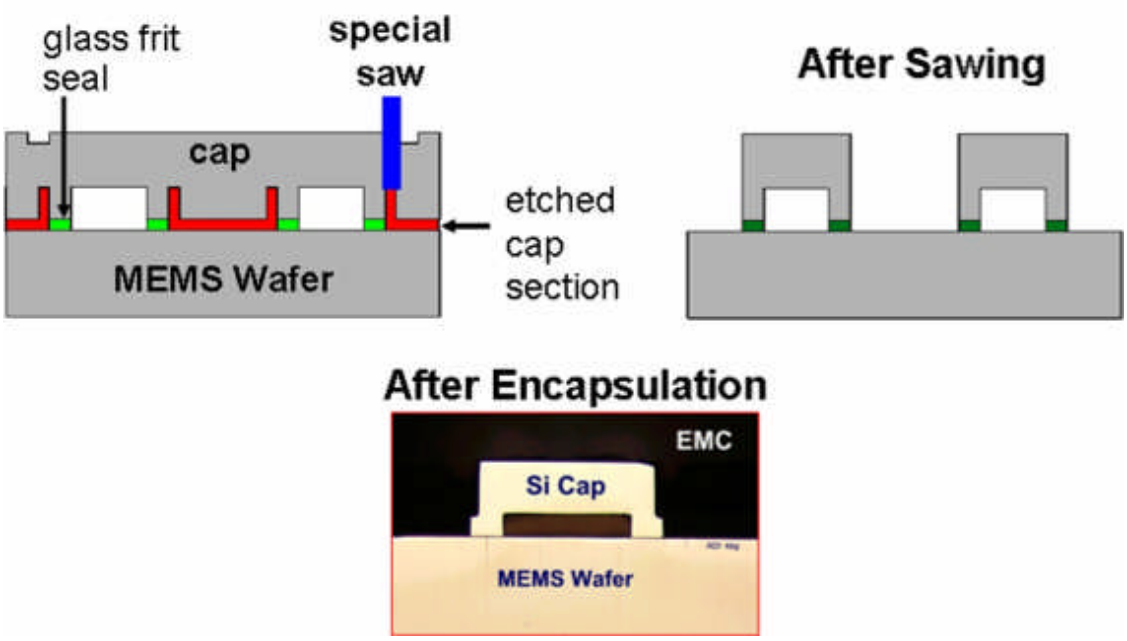

Figure 4 - Capped MEMS Cross-Section (Analog Devices, Inc.)

FUTURE PACKAGING TRENDS

Low-Cost Commodity Packaging

Expect to see a continuation of simple-process, low-cost packages for less-challenging devices. Surface Mount and Area Array are here to stay, and these formats will continue until the need for point-to-point connections is eliminated in a more distant future. While the BGA (Ball Grid Array) will continue for higher I/O chips, the old Land Grid Array (LGA), originally used for leadless ceramic chip carriers (LCCC), is the popular low-cost form factor. However, the structure consisting of flat embedded leads on the bottom of the package is called a QFN (**Q**uad **F**lat pack **N**o-lead) in the "modern" organic version. Cost is reduced by over-molded an entire array of packages, instead of individual ones, and then singulated - an old idea borrowed from ceramic packaging. The only predictable changes are in materials that will adjust to comply with future environmental regulations.

CPU Packages

More than a decade ago, the computer chip industry added so many I/Os to ever-smaller chips that wire bonding became a poor option. The solution was the old IBM direct chip attach (DCA) process now referred to as flip chip. CPUs will continue to use DCA far into the future. It remains to be seen whether some of the "chip-first" CPU packages, like Intel's BBUL (Bumpless Build-Up Layer) will gain popularity in the future. The chip-first design, probably credited to GE, is still a DCA configuration. CPU's with thousands of I/Os will continue to be directly connected to the package, whether by flip chip in package (FCIP) or chip-first constructions. But what about *disruptive technology*?

Ask why we need so many I/Os for computer chips and the answer comes down to *"we need more signals"*. But electrons are rather poor *messengers* and that's the problem. If we used only electrons to carry Internet messages, a web page might take an hour to download. The fleet-footed messenger of the Internet (for long haul and metro loops) is the nearly weightless and zero-charge photon. Although data begins as electrons, it's soon converted to photons that are sent over optical fiber that circles the globe as buried- and submarine cables. *Photonic transmission has about 1-million times more bandwidth than electronics over-copper*. There are many reasons for this incredible disparity, but one important factor is the ability to send a large number of different wavelengths over the same optical fiber with no interference. The Internet photonics concept may soon be applied to CPUs. This disruptive technology will bring about paradigm shifts throughout the industry, if it succeeds.

Intel, UC-Santa Barbara (UCSB), and many others, seek to light-link silicon chips to eliminate the copper bottleneck. Intel refers to the technology as "Silicon Photonics" - modulating lasers formed in compound semiconductor layers that are wafer-bonded to silicon electronics with optical elements. The idea is to perform logic and memory functions with traditional electronics, then convert data to light (actually, invisible infrared) to transmit between chips. When light linking eventually succeeds, the package will have very few I/Os, perhaps only power and ground, but will require optical pathways, like windows and fiber optic ports. Expect new CPU photon-enabled packages within the next 3 to 6-years.

But what about the predicted *Nanoelectronics Breakthroughs*, listed on most roadmaps? While anticipating a transition to *non-silicon electronics*, whether its nano, molecular, or single-electron, the impact on packaging could be minor. Nearly all *beyond silicon* "architectures" describe transistors. So it won't matter to packaging whether the transistor is silicon or a carbon nanotube (CNT). There will still be chips with I/Os to connect. But here's a caveat. If silicon photonics succeeds, then the new generation of electronics will almost certainly use photonics for data.

Future MEMS and Packaging

Today's MEMS can be viewed as a maturing technology but commercial devices are fairly simple pumps, accelerometers, gyroscopes, microphones, and pressure sensors. Advanced MEMS is just starting to move into the commercial sector after considerable efforts by industry, governments, universities and consortia [4]. Emerging products include energy devices, like micro-turbines and micro-fuel cells, Bio- and Medical-MEMS, that will handle fluids, and all kinds of sensors and analyzers. Later, we can anticipate *lab-on-chip* and *pharmacy-on-chip systems* that will run tests and produce materials. The arrival of advanced MEMS chips, needing more than electrical connectivity, will require sophisticated packaging to handle gases, fluids and nano-particles. We'll need fluidic couplings; the package of the future might be entirely manufactured using MEMS fabrication processes (see Figure 5).

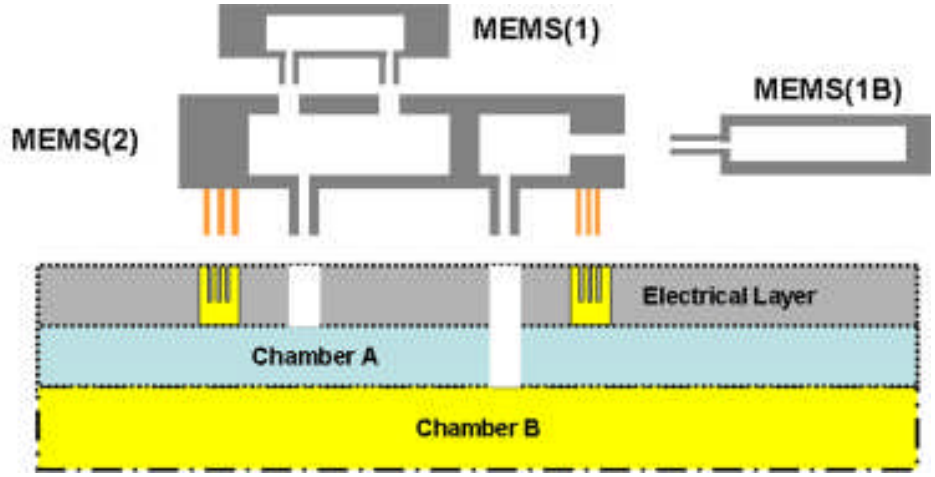

Figure 5 - Package with Fluidic Couplings for MEMS [5]

CONCLUSIONS & PREDICTIONS

Future packaging will fall into two broad classes, low-cost simple, like the QFN, and advanced device/application-specific driven by function and performance. While the old theme song of *faster, smarter, cheaper*, may still be applied to chips, it won't fit packaging without a re-write. The leadless overmolded 5-cent package (QFN) will march to *"cheaper"*, but *faster, smarter* will take on new meaning. Faster will no longer mean clock speed, but will refer to photonic chips - and nothing is faster than light. Smarter can be applied to newer chips that go beyond electrons to handle mechanics and optics, and all the combinations. The old phase *"Shrink the world onto a chip"* can become valid as we learn how to shrink great machines from our macro-world down to chip-size. The day may come when your doctor will again make house calls, by using wireless, and the tele-medic will access your "wellness" using biochips, and your body-roving "bots" will be re-programmed to deal with situations before it becomes a health problem.

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